REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

In the Office Action Summary, the Examiner checked box 13, acknowledging a claim of foreign priority. However, no claim of foreign priority has been made in this case. In a preliminary amendment dated 10/11/2001, a claim for domestic priority was made. Applicant hereby requests acknowledgement of the claim for domestic priority under 35 U.S.C. § 119(e).

Claims 1-22 are pending in this case. Claim 1 is amended herein.

The Examiner rejected claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11 under 35 U.S.C. § 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Tsai et al. (U.S. 446).

Applicant respectfully submits that amended claim 1 is patentable over the AAPA in view of Tsai as there is no disclosure or suggestion of depositing a metal layer using physical vapor deposition, performing a sputter etch using a low bias after depositing the metal layer, and then, depositing a metal filler to fill the hole. The AAPA teaches forming a liner/barrier, forming a seed layer over the liner/barrier and filling the trench or via with copper. As the Examiner noted, the AAPA does not teach a sputter etch after depositing the metal layer. Tsai, likewise, does not teach a sputter etch after depositing a metal layer in the hole. Tsai teaches a multi-step HDPCVD process for forming a dielectric layer. In the process of Tsai, a first portion of the dielectric layer (204) is formed, then a sputter etch of the dielectric layer is performed, and then the remaining portion (206) of the dielectric layer is formed. The Examiner argues that the teachings of a sputter etch of the dielectric layer in Tsai would suggest to one of ordinary skill in the art to modify the teachings of the AAPA to form the claimed invention of

performing a sputter etch after depositing the metal layer and before filling the hole with a metal filler. However, Tsai teaches a dielectric rather than metal process and a (dielectric) fill process rather than performing a sputter etch after depositing a metal layer and prior to depositing a metal filler. Furthermore, Tsai teaches the sputter etch as part of a CVD process rather than after depositing a metal layer by PVD. There is no disclosure or suggestion for applying the dielectric, CVD, gap fill process of Tsai to the metal, PVD process of the AAPA at a point between the liner and metal fill process so as to form the claimed invention. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are patentable over the references.

The Examiner rejected claims 12, 13, 14, 15, and 16 under 35 U.S.C. § 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Tsai et al. (U.S. 446).

Applicant respectfully submits that claim 12 is patentable over the AAPA in view of Tsai et al as there is no disclosure or suggestion in the combined references of performing a sputter etch after depositing a liner/barrier layer by PVD, depositing a seed layer over the liner/barrier layer, and depositing a copper layer over said seed layer. The AAPA teaches forming a liner/barrier, forming a seed layer over the liner/barrier and filling the trench or via with copper. As the Examiner noted, the AAPA does not teach a sputter etch after depositing the liner/barrier layer. Tsai teaches a multi-step HDPCVD process for forming a dielectric layer. In the process of Tsai, a first portion of the dielectric layer (204) is formed, then a sputter etch of the dielectric layer is performed, and then the remaining portion (206) of the dielectric layer is formed. The Examiner argues that the teachings of a sputter etch of the dielectric layer in Tsai would suggest to one of ordinary skill in the art to modify the teachings of the AAPA to add a sputter etch of the liner/barrier layer. Applicant disagrees because it would not be clear to one of ordinary skill in the art how to apply the teachings of Tsai to the AAPA. Tsai teaches a sputter etch as part of a multi-step HDPCVD process for

forming a dielectric layer in a gap between conductors, whereas the AAPA does not involve dielectric gap filling. The AAPA involves filling the gap in the dielectric with metal. There is no suggestion to apply the dielectric fill process of Tsai to the metal fill process of AAPA.

Even if there were a suggestion to apply the dielectric fill process of Tsai to the metal fill process of AAPA, this still does not accomplish the claimed invention. This would only accomplish placing a break in the copper metal fill process to perform a sputter etch. The claimed invention requires performing a sputter etch after depositing the liner. There is no disclosure or suggestion in the references as combined for performing a sputter etch after depositing a liner. Furthermore, Tsai teaches performing the sputter etch on a CVD deposited layer rather than a PVD deposited liner. There is no suggestion for applying the sputter etch of a CVD depositing dielectric layer to the PVD deposited metal liner of the AAPA to accomplish the claimed invention of depositing a liner by PVD, then performing a sputter etch and depositing a seed layer and a copper layer. Accordingly, Applicant respectfully submits that claim 12 and the claims dependent thereon are patentable over the references.

The Examiner rejected claims 17, 18, 19, 20, 21, and 22 under 35 U.S.C. § 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Tsai et al. (U.S. 446).

Applicant respectfully submits that there is no disclosure or suggestion in the references of depositing a liner layer in a contact hole by PVD, wherein the liner layer has an overhang portion at a top of the contact hole, performing a sputter etch using a low bias to at least reduce a thickness of the overhang portion, depositing a barrier layer over the liner layer, and depositing a metal filler to fill the contact hole. The AAPA does not teach a sputter etch to reduce a thickness of the overhang portion of a liner layer. Tsai teaches a sputter etch of a dielectric as part of a HDPCVD dielectric gap fill process. Even if the dielectric

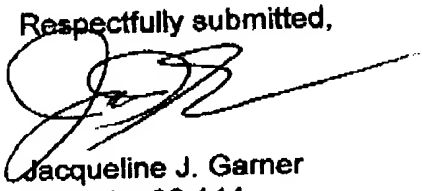
gap fill process of Tsai was applied to the metal fill process of the AAPA, this would not disclose or suggest the claimed invention. It would not disclose or suggest a sputter etch to reduce a thickness of the overhang portion of a liner layer, much less a liner layer deposited by PVD. Accordingly, Applicant respectfully submits that claim 17 and the claims dependent thereon are patentable over the references.

The other references cited by the Examiner have been reviewed, but are not felt to come within the scope of the claims as amended.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made.**"

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,



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Version with Markings to Show Changes Made

Claim 1 is amended as follows:

1. (amended) A method of fabricating an integrated circuit, comprising the steps of:

forming a dielectric layer over a semiconductor body;

forming a hole in said dielectric layer;

depositing a metal layer over said dielectric layer including in said hole using physical vapor deposition;

performing a sputter etch using a low bias after said step of depositing the metal layer; and

then, depositing a metal filler to fill said hole.